IN THE CLAIMS:

Please amend claims 1-4 and 6-15 as follows:

1. (Currently Amended) A data processing device including a set-associative cache memory capable of performing associative operation ~~using~~ by sequentially comparing tag information contained in an access address signal with tag information [[for]] contained in each of ways of a ~~an indexed~~ cache line which is selected as an information storage area with lower bits of the access address signal, said cache memory comprising:

way prediction means for ~~performing~~ predicting one of the ways of the cache line as a matching way ~~selection based on the prediction~~ in parallel with the associative operation;

generation means for generating way selection determining information based on the associative operation using [[the]]a subsequent access address signal during a penalty cycle which is caused by a prediction miss of said way prediction means; and

control means for ~~making a way selected for~~ selecting one of the ways of a cache line, which is selected as an information storage area with lower bits of the subsequent access address signal, as a matching way for the subsequent access address signal after the penalty cycle ~~on the basis of~~ using the way selection determining information.

2. (Currently Amended) The data processing device according to claim 1, wherein said control means ~~makes a way selected on the basis of~~ selects the matching way for the subsequent access address signal using the way selection determining information instead of ~~the~~ prediction by said way prediction means.

3. (Currently Amended) The data processing device according to claim 1, wherein said control means controls rewriting of prediction result information obtained by said way prediction means and corresponding said prediction result information to the way selection determining information.

4. (Currently Amended) A data processing device including a set-associative cache memory capable of performing associative operation ~~using~~ by sequentially comparing

tag information contained in an access address signal with tag information [[for]] contained in each of ways of a ~~an indexed~~ cache line which is selected as an information storage area with lower bits of the access address signal, said cache memory comprising:

instruction means for switchably instructing either of a first operation mode for ~~making a way selection~~ selecting a matching one of ways of a cache line according to [[the]] a result of the associative operation and a second operation mode for ~~making a way selection~~ predicting a matching one of ways of a cache line based on [[the]] prediction conducted in parallel with the associative operation.

5. (Original) The data processing device according to claim 4, further comprising a CPU connected to said cache memory, wherein said instruction means is register means accessible by said CPU.

6. (Currently Amended) The data processing device according to claim 1, wherein the associative operation ~~is to compare predetermined address information contained in access address information with the tag information for each way of the indexed cache line and~~ generates an association result signal ~~indicative of~~ which indicates an association hit or association miss on a way basis.

7. (Currently Amended) The data processing device according to claim 1, wherein ~~the prediction by~~ said way prediction means ~~is processing for determining~~ determines according to way selection history information the least previously selected one of the ways as a ~~selected~~ matching way ~~on the basis of way selection history information~~ for each cache line.

8. (Currently Amended) A data processor including a set-associative cache memory capable of performing associative operation ~~using~~ by sequentially comparing tag information contained in an access address signal with tag information [[for]] contained in each of ways of a ~~an indexed~~ cache line which is selected as an information storage area with lower bits of the access address signal, and a CPU connected to the cache memory, said cache memory comprising a plurality of way and cache control means, wherein

said cache control means predicts one of the ways of the cache line as a matching way ~~makes a way selection based on the prediction~~ in parallel with the associative operation in response to the access operation of said CPU, generates way selection determining information based on the associative operation using a subsequent access address signal during a penalty cycle caused by a prediction miss or cache miss, in which a ~~predictively selected~~ predicted matching way does not match [[the]]a result of the associative operation, on the basis of the associative operation using the subsequent access address, and ~~performs control for making a way selected for~~ selects one of the ways of a cache line, which is selected as an information storage area with lower bits of the subsequent access address signal, as a matching way for the subsequent access address signal after the penalty cycle ~~on the basis of~~ using the way selection determining information.

9. (Currently Amended) The data processor according to claim 8, wherein said control means ~~makes a way selected on the basis of~~ selects the matching way for the subsequent access address signal using the way selection determining information instead of ~~the~~ prediction by said way prediction means.

10. (Currently Amended) The data processor according to claim 8, wherein said control means controls rewriting of prediction result information obtained by said way prediction means and corresponding said prediction result information to the way selection determining information.

11. (Currently Amended) The data processor according to claim 8, wherein said cache control means issues ~~an instruction of~~ an external memory access signal ~~to the subsequent access cache miss~~ during the penalty cycle caused by the prediction miss.

12. (Currently Amended) The data processor according to claim 8, wherein said cache control means includes storage means for storing way selection history information on a cache line basis, and the history information is ~~information~~ used for ~~determining~~ predicting a way corresponding to the least recently accessed information as a ~~selected~~ matching way.

13. (Currently Amended) The data processor according to claim 8, wherein said cache control means includes storage means for storing way selection history information on a cache line basis and updates the history information ~~so that~~ to provide the latest access way ~~selected from~~ of the ~~indexed~~ cache line [[can]] to be predicted as a matching way ~~specified in a prediction process to be performed~~ later.

14. (Currently Amended) The data processor according to claim 8, wherein said cache control means includes storage means for storing way selection history information on a cache line basis and reads out the history information from said storage means according to the lower bits of the access address signal ~~information for indexing the cache line~~ to ~~perform a predictive selection of~~ predict a matching way ~~based on~~ using the read-out history information.

15. (Currently Amended) The data processor according to claim 8, wherein said cache control means judges~~, on the basis of~~ from the tag information contained in ways of the ~~indexed~~ cache line[[,]] whether a cache miss or prediction miss occurs ~~in the way selection process~~, reselects a matching way in response to a judgment that a cache hit ~~and a judgment result of a~~ or prediction miss occurred while updating [[the]] history information corresponding to the cache line ~~to be accessed~~, and instructs an external access in response to the judgment result ~~of the prediction miss~~ so ~~that~~ as to replace the cache line ~~to be accessed will be replaced~~ while updating the history information corresponding to the cache line ~~to be replaced~~.

16. (Original) The data processor according to claim 8, wherein said data processor is formed on a semiconductor chip.